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A 8 mW 72 dB $\Sigma\Delta$-modulator ADC with 2.4 MHz BW in 130 nm CMOS

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Abstract A double-sampling split $\Sigma\Delta$-ADC with bi-linear integrators and a 7-level quantizer is presented. It achieves third order noise shaping with a second order modulator through quantization noise-coupling. The modulator is integrated in a 130 nm CMOS technology. For a clock frequency of 48 MHz and an over-sampling ratio of 20 (2.4 MHz signal bandwidth), it achieves 72 dB DR and 68 dB SNR. The prototype consumes 8 mW from a 1.2 V voltage supply.

Keywords Analog-to-digital converters · double sampling · $\Sigma\Delta$-modulation · noise-coupling · 130 nm CMOS technology

1 Introduction

Wide-band $\Sigma\Delta$-modulation requires a low oversampling ratio (OSR) in combination with high-order noise shaping and multi-bit quantization. In double-sampling $\Sigma\Delta$-modulators, the outputs of the switched capacitor (SC) circuits are updated during both clock phases, doubling the sampling frequency to twice the master clock frequency. Thus for the same power budget, the OSR is doubled. In [1],[2] an enhanced split-architecture $\Sigma\Delta$ ADC is presented. Through the use of noise-coupling the effective noise shaping order is increased. This can lead to a significant reduction in power consumption for low-order modulators [3].

In this paper, we combine double-sampling with cross noise-coupling for a fully integrated prototype.

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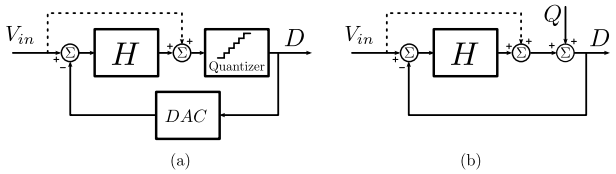


Fig. 1 (a) A $\Sigma\Delta$-modulator and (b) the linearized model.

Section 3 explains the modulator architecture. The circuit level design is discussed in section 4. Measurement results for the integrated prototype are presented in section 5.

2 System Level Design

Fig. 1(a) shows the conceptual diagram of a $\Sigma\Delta$- modulator. The quantizer is embedded in a control loop with loop filter H. The digital output D of the quantizer is fed back to the input of the filter via a digital-to-analog converter (DAC). A common analysis for this system is shown in Fig. 1(b). Here, the quantizer is modelled as an additive white noise contribution Q and the D/A-converter for the feedback path is assumed to be ideal. Fig. 1 also shows an additional feed-forward path from the input signal V_{in} towards the input of the quantizer (dashed line) [4]. In this case, the digital output D of the complete system can be written as:

$$D(z) = V_{in}(z) + NTF(z)Q(z) \tag{1}$$

Here, $NTF(z)$ corresponds to the noise transfer function. The main building block in the loop filter H is an integrator. The magnitude of the loop filter will be high in the low-pass signal band, but low outside the signal band. This way the NTF will be nearly zero in the signal

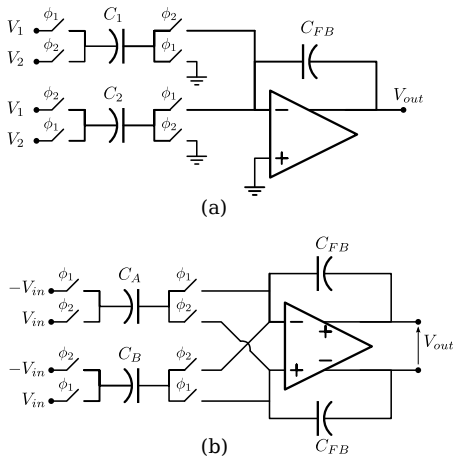


Fig. 2 (a) A conventional and (b) a fully-floating bilinear double-sampling integrator.

band but not outside the signal band. The quantization noise is thus shaped outside the signal band and the output has a very high signal-to-noise-plus-distortion ratio (SNDR) within the signal band.

2.1 Double-Sampling

The efficiency of SC-circuits can be doubled easily by using double-sampling techniques. Fig. 2(a) shows a conventional double sampling integrator with 2 input signals V_1 and V_2. The capacitors C_1 and C_2 are equal. If $V_2 = -V_1$ this circuit performs a bilinear integration:

$$V_{out} = \frac{C_1}{C_{FB}} \frac{(1+z^{-1})}{(1-z^{-1})} V_1(z) \tag{2}$$

However, the conventional double-sampling integrator shown in Fig. 2(a) will suffer from quantization noise folding due to mismatch between capacitors C_1 and C_2. Noise folding will transform signals around the Nyquist frequency ($f_s/2$) towards DC, and as such will degrade the performance of the modulator [5]. Fig. 2(b) shows an alternative circuit that performs a bilinear integration (eq. 2) [6]. For this circuit, it can be shown that mismatch between C_1 and C_2 will not lead to noise folding.

However, because of the bilinear factor $(1+z^{-1})$ in the numerator of eq. (2), the modulator architecture should be modified [7]. The modified architecture for a 2^{nd} order modulator is shown in Fig. 3. The fully floating bilinear integrator is used here for the critical DAC feedback branches, as only this signal path contains signals around the Nyquist frequency. The modulator also shows an additional parameter b_3. This gives the necessary freedom to design the NTF at will [7].

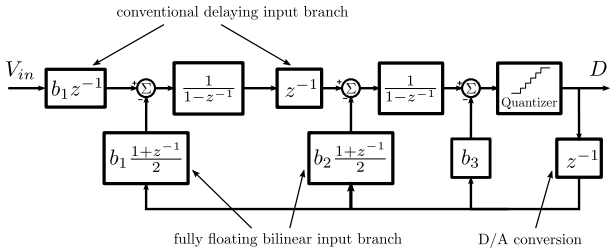


Fig. 3 A modified modulator architecture with bilinear integrators.

2.2 Cross Noise-Coupling

In a split architecture $\Sigma\Delta$ A/D converter, a single modulator is split into two identical halves (Fig. 4). As the two resulting modulator loops have capacitors half the size of those in the original modulator, the total power dissipation and chip area will essentially remain the same. Each modulator loop processes the same input signal independently of the other loop. The two outputs are then combined to generate the total average output signal D_{av}. Since thermal as well as quantization noise are uncorrelated between the two loops, the SNR performance of the split modulator is the same as for the original single modulator.

The noise added by the quantizer can easily be determined by taking the difference between the output and the input of the quantizer. In [1,2] cross noise-coupled split $\Sigma\Delta$-modulator architectures are presented. In such an architecture, the noise of one loop is injected into the other loop as shown in Fig. 4 (dashed line). Applying a linear model to both modulator loops, the outputs from the loops can be obtained:

$$D_a(z) = V_{in} + NTF_a(z)(Q_a - z^{-1}Q_b)$$
$$D_b(z) = V_{in} + NTF_b(z)(Q_b - z^{-1}Q_a)$$

Assuming the NTFs of both modulators are equal, the output signal of the whole structure can be written as:

$$D_{av}(z) = \frac{D_a + D_b}{2}$$
$$= V_{in}(z) + (1-z^{-1})NTF(z)\frac{Q_a(z) + Q_b(z)}{2}$$

The noise shaping now exhibits an additional differentiation $(1-z^{-1})$. Hence the effective noise shaping is of order $n+1$. The injected quantization noise is uncorrelated with the signals in the receiving loop, and acts as a dither signal. Dithering reduces the harmonic distortion and as such improves the dynamic range.

3 Modulator Architecture

In [8] the optimal system level design for a cross noise-coupled 2^{nd} order double-sampling $\Sigma\Delta$-modulator with

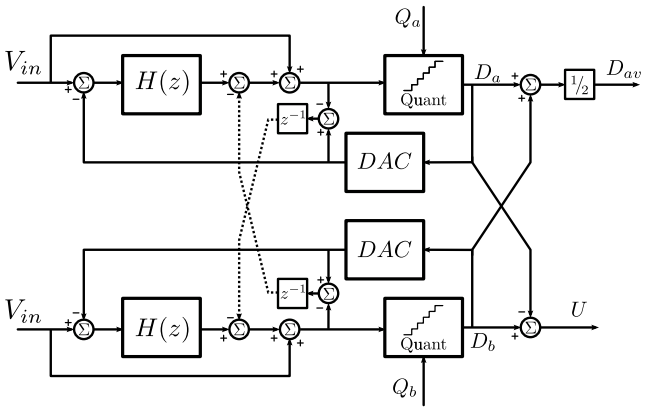


Fig. 4 A split $\Sigma\Delta$-modulator with cross-coupled noise injection.

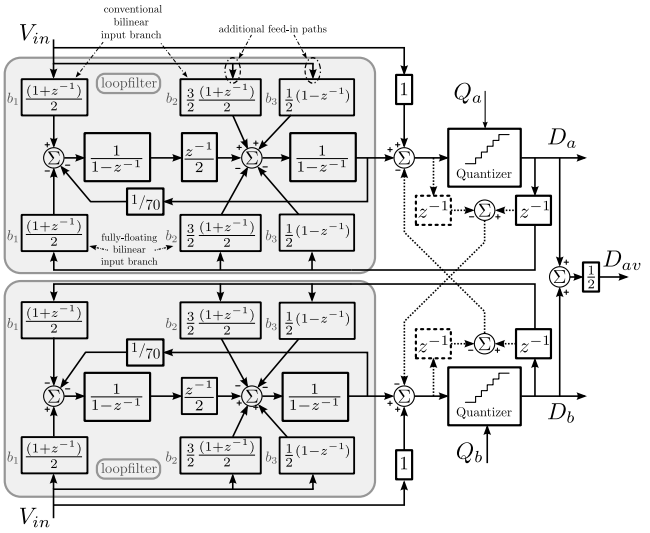


Fig. 5 The implemented modulator architecture.

bilinear integrators is discussed. It is shown that a good choice for the modulator parameters is:

$$b_1 = \frac{1}{2}, b_2 = \frac{3}{2}, b_3 = \frac{1}{2} \tag{3}$$

The final modulator architecture is shown in Fig. 5. The loop filter ($H(z)$ in Fig. 4) consists of a cascade of two integrators with distributed feedback, similar to Fig. 3. Local feedback around the two integrators is used to optimize the NTF zeros. Additional feedin paths for the input signal V_{in} towards internal nodes of the loop filter reduce the output swing of the integrators and as such relaxes the requirements on the operational amplifier design [8]. The feedback branches for the output signal are implemented with a fully-floating bilinear integrator, while the input signal V_{in} is sampled with a conventional (non-floating) bilinear input branch. The coefficient b_3 is implemented as a feed-forward branch at the 2^{nd} integrator (hence the factor $(1 - z^{-1})$).

For a 7-level quantizer and an OSR of 20, system level simulations show that a signal to quantization noise ratio (SQNR) of 85 dB can be reached.

4 Prototype Design

The modulator is integrated in a 130 nm CMOS process with a supply voltage of 1.2 V. In this technology, 2 different types of MOS-transistors are available, high-speed (HS) and low-leakage (LL). The LL-devices show a larger threshold voltage, lower leakage current and a larger gain for a single stage.

All switches are implemented with HS-transistors. For the input-sampling switch a standard CMOS transmission gate is used and the total input-sampling capacitance is 600 fF.

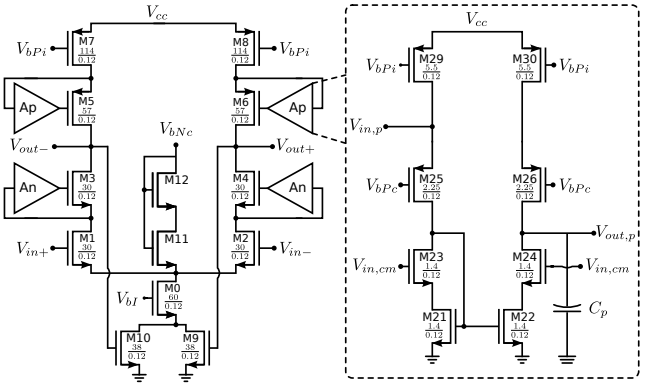


Fig. 6 The circuit for the operational amplifier used in the integrators.

4.1 Operational Amplifiers

The operational amplifier used for the integrators is shown in Fig. 6. In this op-amp circuit all transistors are LL-devices, except for M9 and M10, which are HS-transistors. Operating in triode region, M9-M10 regulate the output common-mode voltage by adjusting the bias current through M0. Because of the low output swing of the integrators, a telescopic cascode op-amp is chosen [8]. System level simulations showed that a DC-gain of at least 55 dB was necessary. To achieve this high gain the cascode transistors are boosted with a high-swing low-voltage regulation amplifier [9]. The booster for the PMOS cascode is also shown in Fig. 6. To attain an accurate settling behaviour, the boosters are band limited by adding small capacitors in their outputs.

4.2 Active Adder

For the implementation of the quantization noise coupling, an active adder is needed at the quantizer input. Fig. 7(a) shows a straightforward double-sampling SC-implementation for this adder. To simplify the figure, only the input branches of the adder that implement the noise-coupling are shown, the analog input of the quantizer of the other loop (V_{Qin}) and the digital output of the other loop ($D = \sum d_i$). All capacitors shown in this figure have the same capacitance and the indices a and b represent the two different modulator loops. Each op-amp has two input branches and two feedback capacitors with altered clock phases (ϕ_1 and ϕ_2). Capacitor $C_{2,a}$ samples the input of the quantizer of the other modulator loop when ϕ_1 is active. During the next active phase of ϕ_2, $C_{2,a}$ is switched between the adder-input and the output of the quantizer of the other loop, $D_b = \sum d_{i,b}$. The net result on the feedback capacitor $C_{FB2,a}$ is $z^{-1}(D_b - V_{Qin,b}) = z^{-1}Q_b$. During ϕ_1, $C_{FB2,a}$ is reset to ensure the correct operation of the adder. $C_{1,a}$ and $C_{FB1,a}$ perform the same operation with altered clock phases.

An improved circuit that performs the same summation is shown in Fig. 7(b). In stead of resetting the feedback capacitor C_{FB1}, the same capacitor is used as feedback capacitor in the adder of the other modulator loop during the next clock phase. Since the voltage stored on C_{FB1} during ϕ_1 is equal to $V_{Qin,a}$, the feedback capacitor performs the summation of $V_{Q,in1}$ at the input of the quantizer in the other modulator loop. This way the capacitive load of the op-amp is halved.

For the active adder a folded cascode op-amp is used to attain the differential full-scale of $\pm 600\,\mathrm{mV}$ at the input of the quantizer. Gain boosting and common mode feedback are done in a similar way as in the telescopic op-amp shown in Fig. 6.

4.3 SC-implementation

The SC-circuit for one modulator loop is shown in fig.8. The dashed lines implement the coupling between the 2 modulator loops. Digital signal busses are drawn with a thick line. The digital output D of the loop is converted by a CMOS selection logic into selection signals for the switches implementing the D/A-conversion. The selection signals for b_3 are different from the selection signals for b_1 and b_2, as b_3 is implemented as a feed forward branch, while b_1 and b_2 are bilinear input branches

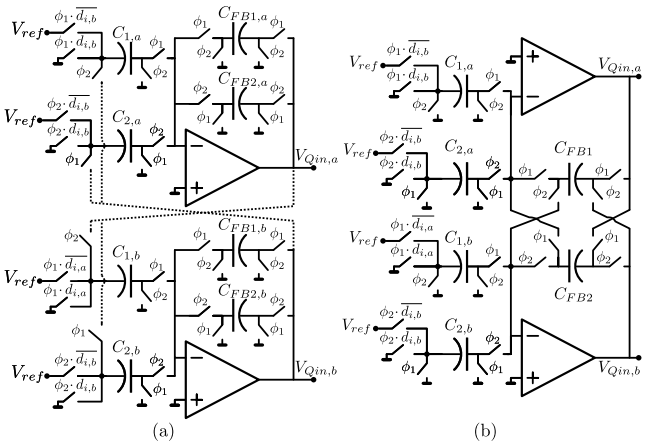
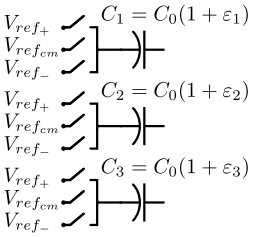


Fig. 7 (a) A double sampling adder circuit and (b) an adder with reduced load capacitance.



DAC level #	C_1	C_2	C_3	actual level
6	+	+	+	$3+\varepsilon_1+\varepsilon_2+\varepsilon_3$
5	+	+	cm	$2+\varepsilon_1+\varepsilon_2$
4	+	cm	cm	$1+\varepsilon_1$
3	cm	cm	cm	0
2	−	cm	cm	$-1-\varepsilon_1$
1	−	−	cm	$-2-\varepsilon_1-\varepsilon_2$
0	−	−	−	$-3-\varepsilon_1-\varepsilon_2-\varepsilon_3$

Fig. 9 Mismatch of the DAC-capacitors and the corresponding DAC-levels.

4.4 DAC calibration

Mismatch in the DAC capacitors is unavoidable. Due to this, the actual DAC level will deviate from its nominal value. This phenomenon is illustrated in Fig. 9. As a result, the relationship between the digital input value of the DAC and the corresponding output level will be non-linear. Since this DAC is used in the feedback path of our $\Sigma\Delta$ modulation ADC, this capacitor mismatch will in the end lead to ADC distortion [10]. A traditional way to solve this problem is to linearize the feedback DAC by the use of a dynamic element matching (DEM) [10] technique. Here, Data-Weighted-Averaging (DWA) is the simplest (and most popular) variant. However, in our double-sampled modulator, this technique is nearly impossible to implement due to the stringent time budget. Indeed the quantizer is strobed at the falling edge of each clock phase, while the DAC is updated at the rising edge of the following clock phase. This way the DWA selection signal should be calculated within the non-overlap between the two clock phases. Obviously, this is almost unfeasible.

Another way to counteract the non-linearity of the DAC capacitors is to use digital calibration [11]. Here the actual DAC output levels are stored in a digital look-up table (LUT). During the normal operation, the

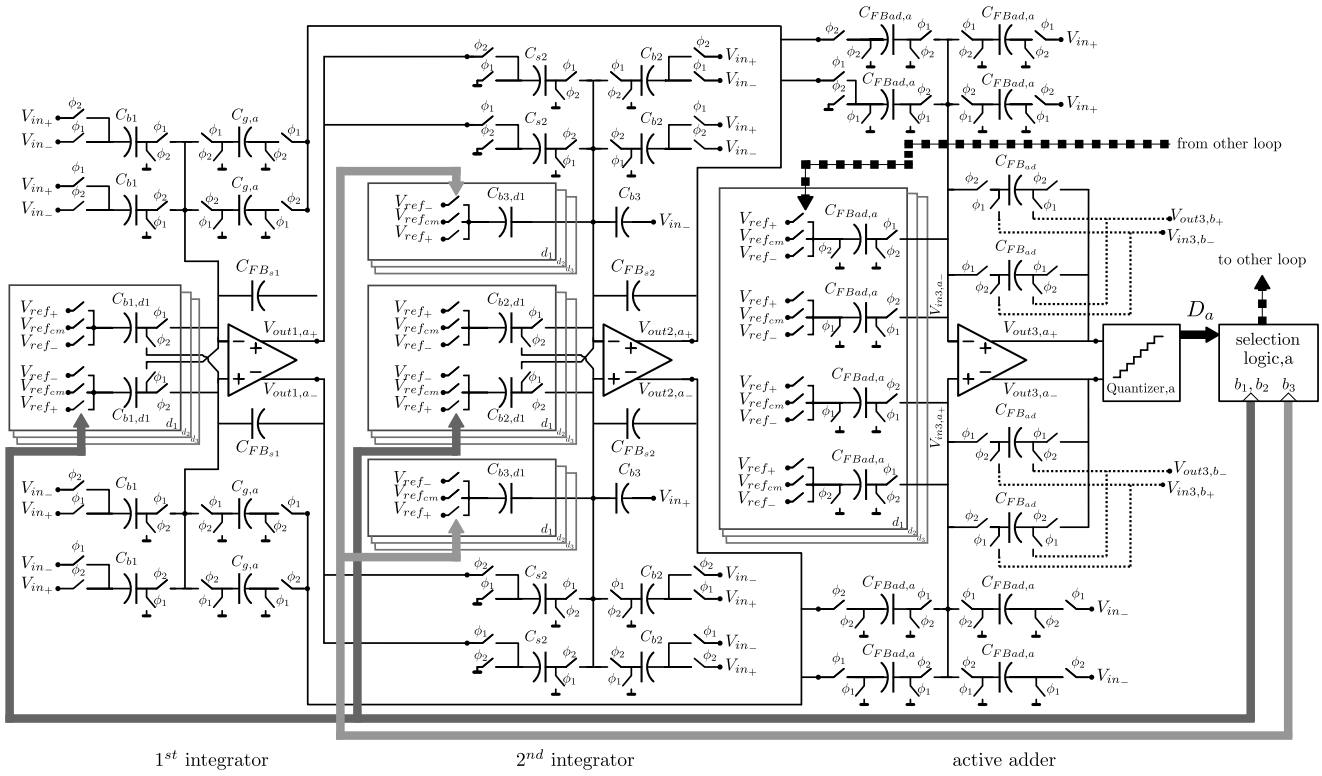


Fig. 8 SC-implementation of the modulator architecture.

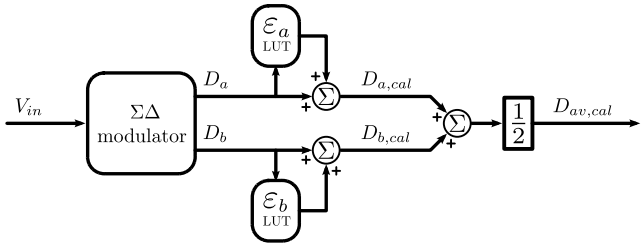


Fig. 10 The calibration scheme.

calibrated output D_{cal} is obtained from the look-up-table. In our case of a fully differential 7-level DAC this look-up table contains three error terms. Since there are two feedback DAC's in our split $\Sigma\Delta$ ADC, we need two of such look-up tables. The resulting structure is shown in Fig. 10. It is clear that this calibration setup corresponds to a nearly negligible amount of additional hardware. Moreover, the calibration is not in a timing critical signal path and hence is not subject to particular timing constraints. In our prototype the look-up table is not integrated in the chip and implemented in software.

Obviously, the accuracy of such a calibration depends on how accurately the values in the look-up table correspond to the actual DAC-errors. In this prototype, the values for the look-up table are first determined in an offline LMS calibration cycle (which is further out of the scope of this manuscript). Then the calibration values are stored in memory for use during the normal operation (shown in Fig. 10). Clearly, this approach cannot correct drifting due to e.g. thermal effects or aging. If this is expected to be a problem, techniques for continuous (online) calibration such as [12] can be used. Such techniques can also successfully correct drifting DAC values, but this was not considered necessary in our case of a switched capacitor DAC and hence no further attention was given to this option.

5 Measurement Results

A prototype that incorporates the above described techniques was designed and submitted for fabrication. Unfortunately, the first silicon samples that we received were subject to a fabrication error. Due to this fabrication error, all the transistors were out of spec. As a result, sampling switches and clock drivers suffered from inadequate drive strength. Still these first samples were fully functional $\Sigma\Delta$ ADC's (be it at a reduced speed and with increased distortion) and their performance was reported in [13]. The measurements reported in this manuscript are from a second batch of samples which is fully compliant now.

Fig. 11 shows a microscope photograph of the prototype chip. Fig. 12 shows a measured spectrum (21K

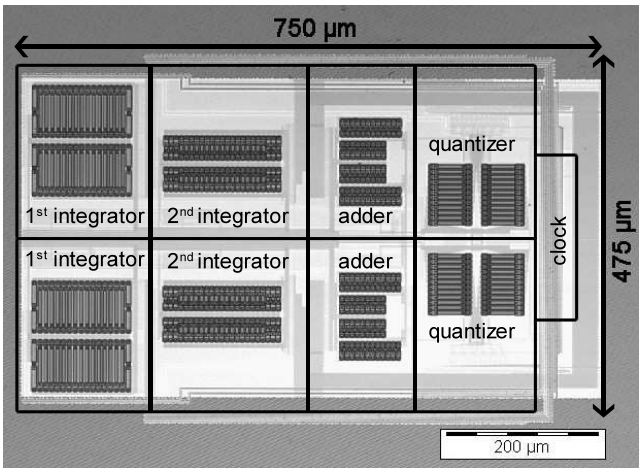


Fig. 11 Microscope photograph of the integrated $\Sigma\Delta$-ADC.

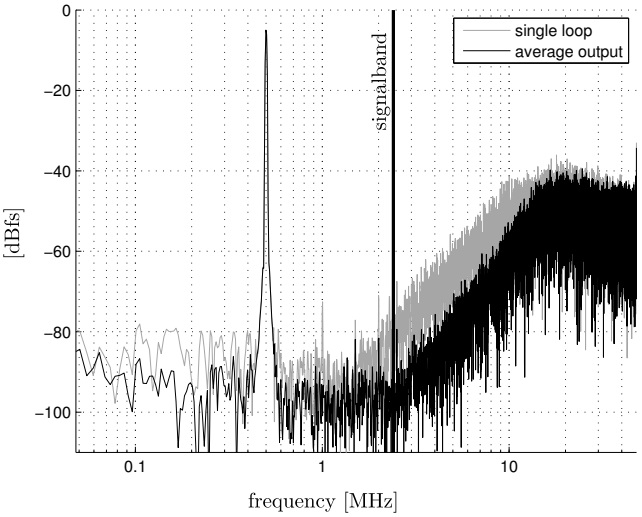


Fig. 12 Measured output spectrum for a -5 dBFS 501 kHz input tone.

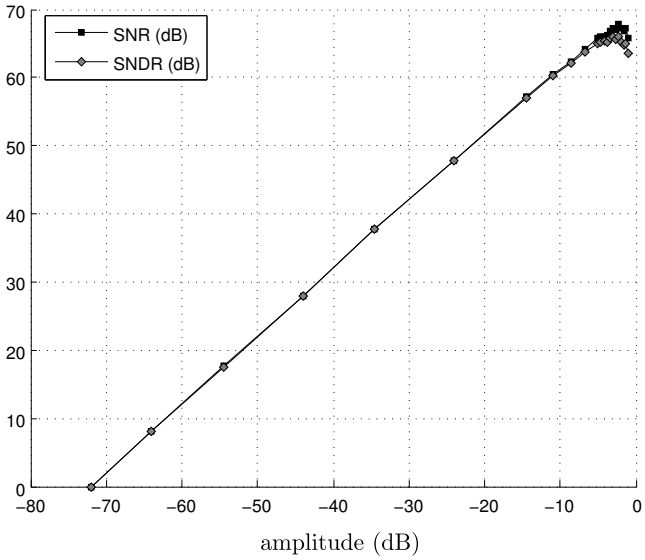


Fig. 13 SNR and SNDR vs. input amplitude for a 501 kHz input tone.

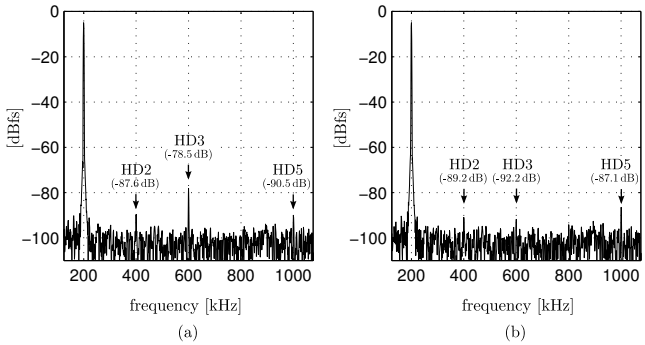


Fig. 14 Measured output spectrum for a -5 dBFS 201 kHz input tone without (a) and with (b) calibration.

FFT - blackman window) for a sinusoidal input signal of 501 kHz and a -5 dB amplitude relative to fullscale (dBFS) after calibration. The greyed spectrum corresponds to a single modulator, whereas the black spectrum corresponds to combined spectrum of both coupled modulators. It is clear that the noise-coupling works as expected and greatly enhances the noise shaping. For this measurement, the 3rd harmonic is at -82.4 dB and the 4th harmonic is at -82 dB. Fig. 13 shows the SNR and SNDR as a function of input signal amplitude (measured at 501 kHz). The peak SNR is 67.8 dB for -2.2 dBFS and the peak SNDR is 66.1 dB for -3 dBFS. The dynamic range is 72 dB.

The previous measurements were for the case where the digital calibration of Fig. 10 is active. The effect of the digital calibration is illustrated in Fig. 14, where measured spectra with and without digital calibration are shown. Here the signal frequency is chosen such that the 5th harmonic is still within the signal band. In the case without digital calibration (Fig. 10.a) the SFDR is limited by the 3rd harmonic. After calibration (Fig. 10.b) the SFDR improves by 9dB and is now limited by the 5th harmonic which was slightly increased. The resulting distortion is attributed to signal dependent charge injection in the sampling switches.

The high frequency linearity is illustrated in Fig. 15, where the measured spectrum for a two-tone test is shown. Here the two tones are placed near the band edge. For this measurement the digital calibration is activated. From the magnitude of the intermodulation products we can conclude that the distortion increases for higher input frequencies which could indicates that there is tracking distortion in the sampling switches.

The total power dissipation is 8 mW of which 6.4 mW is dissipated in the analog core. Fig. 16 shows a detailed distribution of the power consumption. From the above measurements we can also calculate Walden's figure-of-merit (FOM) [14], defined by $FOM = P/(2 \cdot BW \cdot$

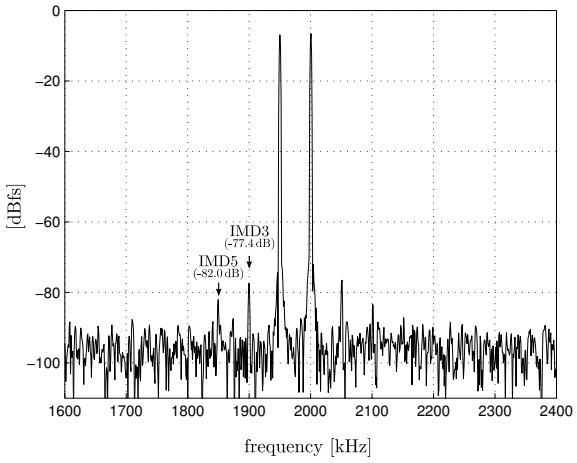


Fig. 15 Measured output spectrum for two -7 dBFS 1.95 MHz and 2 MHz input tones.

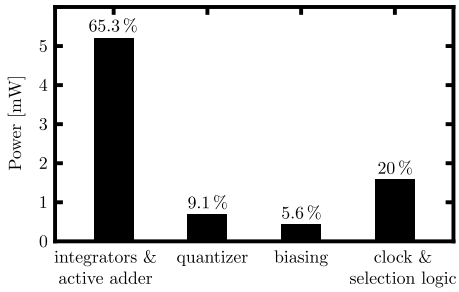


Fig. 16 Power consumption distribution.

2^{ENOB}) ([14]), as 0.5 pJ/conversion-step. It should be noted though, that the relevance of this FOM has been subject to debate [15] and that it is only added here for illustrative purposes.

These measurement results, as well as a comparison with other recent switched-capacitor $\Sigma\Delta$ ADCs are summarized in table 1. From the table it is clear that our prototypes performance compares well with other recent implementations.

6 Conclusion

A split $\Sigma\Delta$-A/D converter architecture combining quantization noise-coupling and double-sampling is presented. By adding cross noise-coupling between the two identical loops of the split second order modulator, the effective noise shaping order is increased to 3. To tackle the problem of quantization noise folding in a double-sampling SC-circuit, a fully floating bilinear input branch is used for the feedback of the D/A-converter. A prototype achieves 72 dB DR and 68 dB SNR over a 2.4 MHz signal band for a power budget of 8 mW.

Acknowledgement

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Table 1 Performance Comparison

Feature	This Work	[16]	[17]	[18]	[19]-A	[19]-B	[20]	[21]
CMOS technology (nm)	130	250	130	180	180	180	180	90
Supply voltage (V)	1.2	1.2	1.2	1.2	24	24	1.8	1.2
Oversampling ratio	20	16	48	16	1.5	1.5	8	20
Signal bandwidth (MHz)	2.4	1.25	1.92	0.625	4.2	2.5	6	1.92
Peak SNDR (dB)	66.1	89	59	74.6	79	81	60.7	65.5
Dynamic range (dB)	72	96	62	77	81	83	62	66
Active area (mm2)	0.36	8.6	0.36	1.92	3.67	3.67	0.32	0.076
Power consumption (mW)	8	44	3.1	3.2	28	15	6.18	6.8
FOM [14] (pJ/conv-st)	0.5	0.64	0.788	0.58	0.48	0.33	0.58	1.17

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